

**AMENDMENTS TO THE CLAIMS**

1. (Canceled)
2. (Previously Presented) An integrated circuit device comprising:
  - a plurality of internal circuits for generating a plurality of internal signals, the internal signals used for addressing storage locations and for controlling internal operations;
  - a first selection circuit for receiving the internal signals in response to selection signals corresponding to test information signals;
  - a second selection circuit for receiving output signals from the first selection circuit and output signals from a sense amplifier, and for opening an alternative one of transfer paths for the internal signals and the output signals of the sense amplifier in response to the selection signals; and
  - a data output buffer for transferring output signals from the second selection signals externally from the integrated circuit device through data input/output pads, the data input/output pads being shared by the internal signals and the output signals from the sense amplifier.
3. (Currently Amended) A method for monitoring internal signals in an integrated circuit device having input/output pads, the method comprising ~~the steps of:~~
  - detecting a test mode;
  - selecting a part of internal signals of the integrated circuit device in response to selection signals, the internal signals used for addressing storage locations and for controlling internal operations;

selecting an alternative one of transfer paths of the part of the internal signals and output signals from the integrated circuit device in response to the selection signals; and

transferring the part of the internal signals external to the integrated circuit device

4. (Currently Amended) A method for monitoring internal signals in an integrated circuit device having sense amplifier, a data output buffer, and input/output pads, the method comprising ~~the steps of~~:

detecting a test mode in response to a logical states with external control signals of the integrated circuit device;

selecting a part of internal signals of the integrated circuit device in response to selection signals corresponding to test information signals;

selecting an alternative one of transfer paths of the part of the internal signals and output signals from the sense amplifier in response to the selection signals, the internal signals used for addressing storage locations and for controlling internal operations; and

transferring the part of the internal signals external to the integrated circuit device through the data output buffer and the input/output pads, the data input/output pads being shared by the internal signals and the output signals.

5. (Currently Amended) The device of claim 4 21 wherein the internal signals include row information, column information, and control information.

6. (Currently Amended) The device of claim 4 21 further comprising:  
a test information input circuit configured to send the selection signals to the selection circuit.

7. (Previously Presented) The device of claim 6 wherein the test information input circuit is configured to generate the selection signals in correspondence to the test information signals and a test mode signal.

8. (Previously Presented) The device of claim 7 wherein the test mode signal is in response to dynamic random access memory control information.

9. (Previously Presented) The device of claim 2 wherein the internal signals include row information, column information, and control information.

10. (Previously Presented) The device of claim 2 further comprising:  
a test information input circuit configured to send the selection signals to the selection circuit.

11. (Previously Presented) The device of claim 10 wherein the test information input circuit is configured to generate the selection signals in correspondence to the test information signals and a test mode signal.

12. (Previously Presented) The device of claim 10 wherein the test mode signal is in response to dynamic random access memory control information.

13. (Canceled)

14. (Previously Presented) The method of claim 3 wherein the selecting is based on the detected test mode.

15. (Previously Presented) The method of claim 3 wherein the detecting is based on dynamic random access memory control information.

16. (Previously Presented) The device of claim 3 wherein the internal signals include row information, column information, and control information.

17. (Canceled)

18. (Previously Presented) The method of claim 4 wherein the selection signals also correspond to detected test mode information.

19. (Previously Presented) The method of claim 4 wherein the logical states are based on dynamic random access memory control information.

20. (Currently Amended) The ~~device~~ method of claim 4 wherein the internal signals include row information, column information, and control information.

21. (Previously Presented) A semiconductor memory device, comprising:  
a test detector circuit configured to generate a test signal in response to external control signals;

a selection signal generator circuit configured to receive an address selection signals in response to the test signal and to generate section signals;

a first selection circuit configured to select internally generated signals in response to the selection signals;

a second selection circuit configured to select either data read out from memory cells or an output of the first selector circuit in response to the selection signals; and

an output buffer circuit configured to output an output of the second selector circuit to the outside.